

Programmable Logic Essentials 2nd Edition

Book 1, Combinational Logic

Book 2, Sequential Logic

The second edition is completely revised to increase the focus on FPGAs from a practical programming standpoint. The intent of both volumes continues to be core coverage of only those digital topics that are judged relevant from a modern programmable device perspective.

A much more pleasing layout has been adopted. Each Figure now carries its own alternate explanation that makes the diagrams more self explanatory and useful for review purposes. The efficient “learn by participating” approach, has been maintained and fine tuned. This approach is a very practical one, where concepts are presented intuitively and supported by in-text exercises that confirm understanding as the topics are introduced. All in-text exercises have complete solutions presented at the end of each chapter. The goal is to have the text used daily in the classroom and written in during lectures, and the fold-back coil binding lends itself to this objective. The two volume format keeps the size down to that of a typical coil notebook, which is very handy.

Each chapter includes a pair of assignments, with a complete solution to the first now included for study purposes. In terms of practical programming activities, the focus has shifted to the free down-loadable Altera Quartus II software. The previous coverage of Capilano Computing’s LogicWorks simulation software remains. This software is excellent from a pedagogical standpoint relative to basic concepts.

Previous minimization and discrete gate coverage has been retained only to the extent that the material provides a foundation or perspective. Likewise a minimal coverage of circuit breadboarding is useful because it encourages a thought process that compliments the design process associated with PLDs. CUPL is not a viable language for the programming of CPLDs and FPGAs and has been replaced by Quartus II, Version 9 software. This software being state of the art and commercial allows very high level design, but it is not easy for a student to assimilate while struggling with core digital concepts. It is introduced gradually. in Book 1 and is covered extensively in Book 2 with many interesting projects.

Although a hardware description language (HDL) is not presently covered, concepts are presented in a way that presupposes eventual VHDL coverage. Quartus II is capable of creating Verilog or VHDL files from the graphic files created using the Block Diagram File (bdf) format. In other words, an instructor could have students examine the VHDL files associated with the designs that have been included in these two volumes. It is the author's opinion that it is undesirable to introduce the complexities of an HDL in an introductory digital course.

Because Quartus II is complex, it is desirable initially to take a block diagram/schematic capture approach. This is not as restrictive as one might suppose since Altera has provided a library of parameterized modules. These modules are based on an HDL and by using the Megafuncion Wizard, can be customized as needed. This allows all the circuits associated with previous 74xx series MSI logic to be utilized, not to mention other more powerful functions such as multipliers and RAM.

While it is possible to use Quartus II without a supporting logic hardware kit, the experience would be far from rewarding for obvious reasons. It is therefore strongly recommended that the Altera DE-2 kit be purchased. It is an excellent platform allowing the eventual coverage of very advanced topics such as microcomputer basics and video and audio processing via the soft processor that can be programmed into the Cyclone II FPGA. With its numerous switches, LEDs, 7-segment displays and I/O ports, it more than adequately supports a great variety of laboratory activities including those provided by the Altera University Program.

In summary, the author continues to take a practical approach, presenting core concepts intuitively so that they are well understood in preparation for serious involvement with PLDs and a Hardware description Language.

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74HC02	Quad 2-input NOR	74HC151	8-input MUX
74HC04	Hex Inverter	74HC163	4-bit Mod 16 Counter with Pre
74HC08	Quad 2-input AND	74HC164	S-in, P-out 8-bit Shift Register
74HC10	Triple 3-input NAND	74HC165	P-in, S-out 8-bit Shift Register
74HC32	Quad 2-input OR	74HC194	4-bit Universal Register
74HC74	Dual D Flip-Flop	74HC247	7-segment Decoder-Driver
74HC76	Dual JK Flip-Flop	74HC280	9-bit parity generator/checker
74HC85	4-I/P Magnitude Comparator	74HC283	4-bit Full Adder
74HC86	Quad 2-input XOR		Altera DE-2 FPGA kit I/O, Pin Configuration Information

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